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ABSTRACT OF THE INVENTION

The present invention discloses a novel layout and process for a device with segmented BLM for the I/Os. In a first embodiment, each BLM is split into two segments. The segments are close to each other and connected to the same overlying bump. In a second embodiment, each BLM is split into more than two segments. In a third embodiment, each segment is electrically connected to more than one underlying via. In a fourth embodiment, each segment is electrically connected to more than one underlying bond pad.